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Simulation of Charge Transport in Disordered Assemblies of Metallic Nano-Islands: Application to Boron-Nitride Nanotubes Functionalized with Gold Quantum Dots

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ABSTRACT

In this study, we investigate the charge-transport behavior in a disordered one-dimensional (1D) chain of metallic islands using the newly developed multi-island transport simulator (MITS) based on semi-classical tunneling theory and kinetic Monte Carlo simulation. The 1D chain is parameterized to model the experimentally-realized devices studied by Lee *et al.* [*Advanced Materials* **25**, 4544-4548 (2013)], which consists of nano-meter-sized gold islands randomly deposited on an insulating boron-nitride nanotube. These devices show semiconductor-like behavior without having semiconductor materials. The effects of disorder, device length, temperature, and source-drain bias voltage (V_{SD}) on the current are examined. Preliminary results of random assemblies of gold nano-islands in two dimensions (2D) are also examined in light of the 1D results.

At $T = 0$ K and low source-drain bias voltages, the disordered 1D-chain device shows charge-transport characteristics with a well-defined Coulomb blockade (CB) and Coulomb staircase (CS) features that are manifestations of the nanometer size of the islands and their separations. In agreement with experimental observations, the CB and the blockade threshold voltage (V_{th}) at which the device begins to conduct increases linearly with increasing chain length. The CS structures are more pronounced in longer chains, but disappear at high V_{SD}. Due to tunneling barrier suppression at high bias, the current-voltage characteristics for $V_{SD} > V_{th}$ follow a non-linear relationship. Smaller islands have a dominant effect on the CB and V_{th} due to capacitive effects. On the other hand, the wider junctions with their large tunneling resistances predominantly determine the overall device current. This study indicates that smaller islands with smaller inter-island spacings are better suited for practical applications. Temperature has minimal effects on high-bias current behavior, but the CB is diminished as V_{th} decreases with increasing temperature.

In 2D systems with sufficient disorder, our studies demonstrate the existence of a dominant conducting path (DCP) along which most of the current is conveyed, making the device effectively quasi-1-dimensional. The existence of a DCP is sensitive to the device structure, but can be robust with respect to changes in V_{SD}.

INTRODUCTION

Recent advances in the development of new materials and fabrication techniques have spurred continued interest in further miniaturization of conventional field-effect devices with new device structure designs [1]. Multi-gate architectures have been fabricated that may allow further reduction in the dimensions of classical metal-oxide semiconductor field effect transistors (MOSFET) without degrading the transistor performance [2]. On the other hand, conduction by tunneling in granular metallic systems has been a subject of interest for many years [3,4]. Single-electron transport devices that operate based on tunneling of individual electrons through junctions formed with one or more nanometer-sized islands have been demonstrated, some even operating at room temperature [5,6]. Successful attempts have been made to demonstrate their use as single-electron memory devices and for nanometer-scale displacement sensing [7,8].

This computational study attempts to complement experimental work seeking to elucidate the effects of different factors such as structural disorder on electron tunneling transport [9,11] by beginning to systematically explore the effects of island sizes, inter-island spacings, and conduction channel length on *IV* characteristics [10]. Particular focus is given to modeling charge transport in boron-nitride nantotubes (BNNTs) functionalized with nanometer-size gold islands. The device properties are investigated at low and high biases, and the effects of temperature on the Coulomb blockade and the device threshold voltage are studied. Later, the work is further extended to study the effect of structural disorder on 2D device characteristics that gives an insight into the functioning of experimentally fabricated multi-dimensional devices.

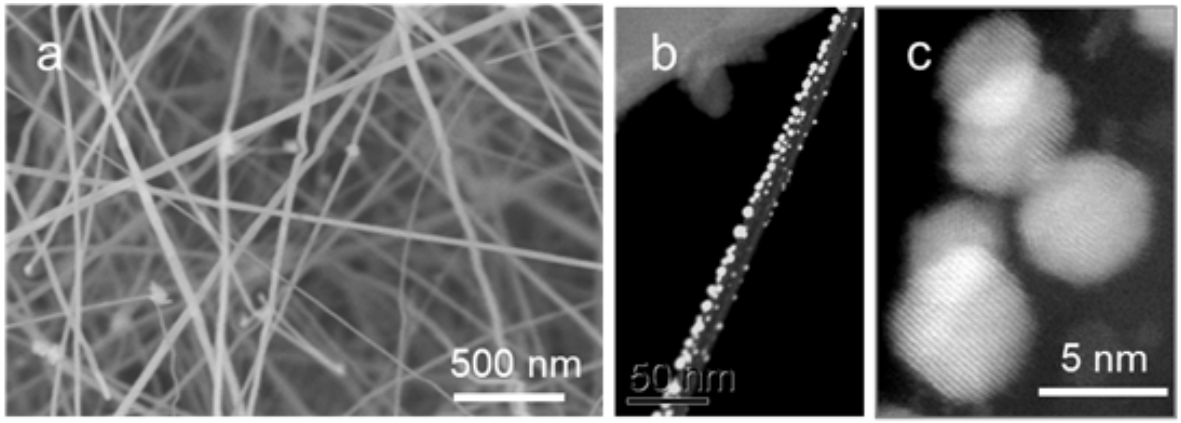

Figure 1. Images of gold quantum dot functionalized boron nitride nanotube s (QDs-BNNTs) obtained by (a) scanning electron microscopy and (b,c) scanning transmission electron microscopy. Reprinted with permission from Lee *et al.* [11]. Copyright © 2013 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

Functionalization of high-quality 20-80 nm diameter BNNTs with gold quantum dots deposited by pulsed laser deposition has recently been demonstrated by Lee *et al.* [11] (figure 1). Without gold-dot functionalization, the BNNTs are excellent insulators, and show currents of less than 10^{-11} A under bias potentials up to 180 V. On the other hand, the gold quantum-dot-functionalized BNNTs (QDs-BNNTs) exhibit room temperature semiconductor-like switching behavior, with turn-on voltages (V_{th}) in the range of 2.0 to 34.0 V, increasing with increasing length (L) of the QDs-BNNT device, where L ranges from 1.29 to 2.37 μm (figure 2).

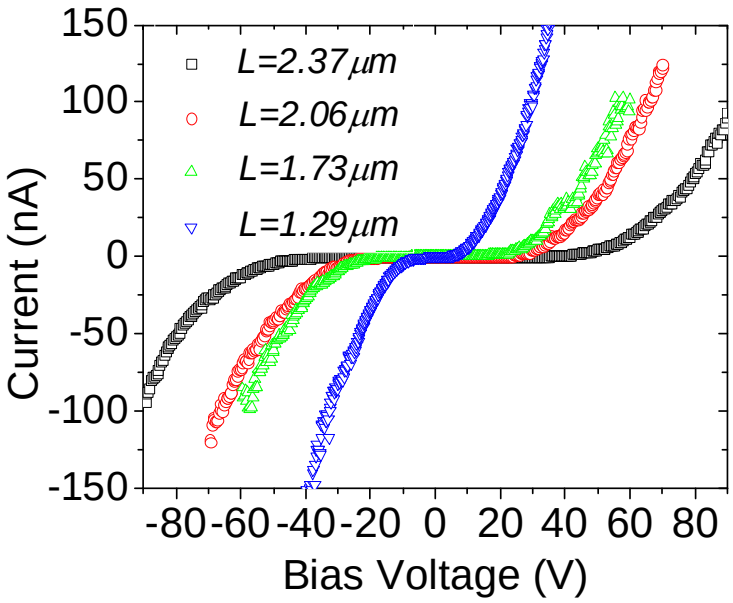

Figure 2. Current-voltage characteristics of QDs-BNNT devices of different lengths demonstrating non-Ohmic behavior, and Coulomb-blockade effects. Data collected using 4-probe scanning tunneling microscopy. Reprinted with permission from Lee *et al.* [11]. Copyright © 2013 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

THEORY AND SIMULATION

Initial investigations were focused on model one-dimensional systems corresponding to the QDs-BNNTs of Ref. 11 (figure 3). The model device consists of a chain of 199 gold islands (200 junctions) between source and drain electrodes. In this study, the BNNT is assumed to play no role other than to geometrically align the islands because of its insulating nature in the absence of gold islands. The radius of each island is randomly selected from a uniform distribution between 3 and 10 nm, while the junction widths are randomly chosen from a uniform distribution in the range of 1 and 5 nm. An island at one end of the chain is selected to be a fixed drain electrode, while the source (ground) electrode is chosen from among the remaining islands in the chain, thus fixing the number of islands in the system (chain) and its length.

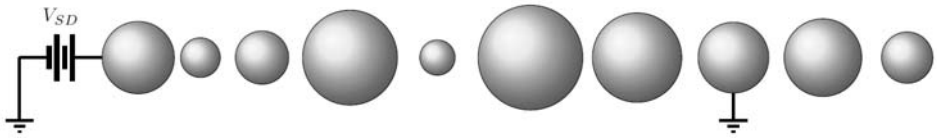

Figure 3. Schematic of the geometrical model of a 1D chain of gold nano-islands with randomly selected island radii and junction widths, deposited on an insulating born-nitride nanotube used for the MITS simulation of systems fabricated by Lee *et al.* [11]. Reprinted with permission from Savaikar *et al.* [10]. Copyright 2013, AIP Publishing LLC.

Conduction in the multi-island devices is modeled using kinetic Monte Carlo simulation methods [12-13] based on tunneling rates that are computed semi-classically (see Ref. 10 for

further details). The probabilities for tunneling between any pair of nearby islands at any given time depend on three primary factors: the charge states of the islands, the voltage drops across the junctions, and the junctions' tunneling resistances. All three of these factors can dynamically vary during the simulation. In particular, in contrast to most models that use tunneling resistances that are fixed throughout the simulation, the tunneling resistances in MITS dynamically vary with the voltage drops across the junctions, both due to the applied voltage bias, and the charge states of the capacitively coupled islands.

The semi-classical approach used for calculating the tunneling rates assumes that (i) the energy spectrum of the conductive islands may be considered continuous (ii) the tunneling time is negligible compared to the time between successive tunneling events, and (iii) coherent tunneling events are ignored [14,15]. For a pair of adjacent islands *i* and *j*, the tunneling rate is given by [14-16].

$$\Gamma_{ij}(\Delta W_{ij}) = \left(\frac{-\Delta W_{ij}}{e^2 R_{ij}}\right)\left[1-\exp\left(\frac{\Delta W_{ij}}{k_B T}\right)\right]^{-1}, \qquad (1)$$

where ΔW_{ij} is the change in the free energy of the system due to the tunneling event, R_{ij} is the tunneling resistance of the junction, e is the electron charge, k_B is the Boltzmann constant, and T is the temperature. As is clear from Eq. 1, ΔW_{ij} and R_{ij} each play key roles in determining the tunneling rates across the device.

Consider first the change in free energy due to the transition, which is given by $\Delta W_{ij} = -eV_{ij} + E_{c,ij}$. This depends on the potential drop V_{ij} that exists across the junction before the transition. V_{ij} in turn depends on the capacitances of the system, which are fixed, and the charge state of the system, which dynamically evolves. The junction charging energy, $E_{c,ij}$, is the energy required for a single electron to tunnel across the junction between the two uncharged coupled islands, *i* and *j*, and depends on all of the capacitances of the system [14-16]. An analytical method employing image charges was used for the calculation of junction capacitances C_{ij} between neighboring islands [18-19], and the dielectric constant of the junction material was taken simply to be 1. Given the self-capacitances and junction capacitances, a capacitance matrix $\boldsymbol{C}$ is constructed that relates $\boldsymbol{Q}$, a vector composed of the charges on the islands, and $\boldsymbol{V}$, a vector composed of the island potentials through the matrix equation $\boldsymbol{Q} = \boldsymbol{CV}$ [15]. As the charge state $\boldsymbol{Q}$ of the device changes, the matrix equation is used to solve for the island potentials.

The tunneling rate for a junction is also dependent on the junction's tunneling resistance R_{ij}, which is a strong function of the device geometry as it increases exponentially with the fixed junction separation d_{ij}. R_{ij} also depends strongly on the height of the energy barrier between the two islands that form the junction. The barrier height depends on the work function of the islands ϕ, as well as the potential drop V_{ij} across them. If eV_{ij} remains small compared to ϕ, it has a negligible effect on the barrier height and R_{ij} would be a constant. Under simulation conditions in which all the junction resistances in a given chain remain constant, the device *IV* characteristics follow a linear behavior for large source-drain voltage biases. However, under high bias conditions, especially where there is a large charge build on some islands, the potential difference between the neighboring islands can be significant compared to ϕ, leading to significant band bending. As a result, the effective barrier height would strongly depend on V_{ij}

and subsequently, R_{ij} would vary significantly with the applied source-drain bias or with the charge state during the course of the simulation. Although a junction's barrier height decreases approximately linearly from one island to the next, in order to simplify the calculations, the tunneling barrier is taken to be of constant height across the width of the junction, but with a reduced height whose variation is given by $\phi_{eff,ij} = \phi - eV_{ij}/2$, a reasonable approximation as long as for each junction $V_{ij} < \phi$ [17]. Thus the tunneling resistances are given by [4]

$$R_{ij} = \left(\frac{h^3}{64\pi^2 m_e e^2}\right)\left(\frac{E_F + \phi_{eff,ij}}{E_F}\right)^2 \frac{\exp\left(2\alpha k_0 d_{ij}\right)}{\phi_{eff,ij}}\left(\frac{\alpha k_0}{r_a}\right)\frac{1}{G_{ij}}\ , \qquad (2)$$

where $k_0 = (2\pi/h)(2m_e\phi_{eff,ij})^{1/2}$, h is the Planck constant and m_e is the free electron mass. α is an enhancement parameter that was taken to be 0.115 to set an overall current scale comparable to that measured by Lee *et al.* [11]. Approximate values of E_F and ϕ for gold have been chosen as 5.5 eV and 4.8 eV, respectively. The average radius of the two spherical islands forming the junction is r_a, and d_{ij} is the closest distance between their surfaces (the junction width). G_{ij} is a purely geometrical factor that takes into account the solid angle subtended by one spherical island at the other across the tunnel junction when considering the current flux [4].

Simulations were carried out using a newly-developed set of MATLAB®-based codes called MITS (Multi-Island Transport Simulator) that is described in detail in Ref. 10. Important features of MITS include the following:

- The system is described by a physical model of islands and electrodes, in contrast to using fixed resistances and capacitances in a circuit model.
- The model is applicable from low to reasonably high V_{SD}. Tunneling barrier heights dynamically change with charge state and V_{SD}.
- All islands within a set proximity limit are capacitively coupled to each other.

To begin a simulation, a physical model of a tunneling device is constructed, consisting of spherical metallic islands arranged in one- or two-dimensions, with desired sizes and spacings. For the modeling of the one-dimensional (1D) QDs-BNNT systems, the capacitances are calculated analytically. For two-dimensional (2D) systems, a finite-element-method of calculating the capacitances has been developed in order to account for the important polarization effects of the metallic islands. The circuit-matrix solver builds the capacitance matrix, by which the charging energies for the transfer of a single electron are calculated across all the junctions in a given chain [14-16]. With the given (fixed) electrode potentials and the known island charges (taken to be zero in the initial system configuration), the capacitance matrix is then used to determine the island potentials. The tunneling resistance solver computes the R_{ij} across all the nearest-neighbor junctions. Once all of the relevant parameters in the system are determined, tunneling rates across the junctions are computed. Following the kinetic Monte Carlo method, a particular tunneling event is randomly selected from among the available events, the corresponding transition is carried out, and the time is updated. Using the system's new charge configuration, the potential drops, the tunneling resistances, and the tunneling rates across all the junctions are recalculated, and the process is repeated for large number of time steps until the current through the device reaches a steady state with satisfactory statistical accuracy.

RESULTS

One-dimensional devices

Current-voltage (*IV*) characteristics at $T = 0$ K for the model 1D device are shown in figure 4. At high biases (figure 4a) the *IV* characteristics are non-Ohmic and vary as $I \propto (V_{SD} - V_{th})^{\zeta}$. The exponent ζ is non-universal and varies between 1 and 3, increasing from 1 with decreasing chain length. For a fixed N, ζ also shows a crossover from a lower value at low bias to a higher value at high bias. The Coulomb blockades and Coulomb staircase (CS) structures are shown for different device lengths in figure 4b. The blockade width and associated threshold voltage V_{th} increase with increasing N. The CS structures are also more pronounced for longer devices.

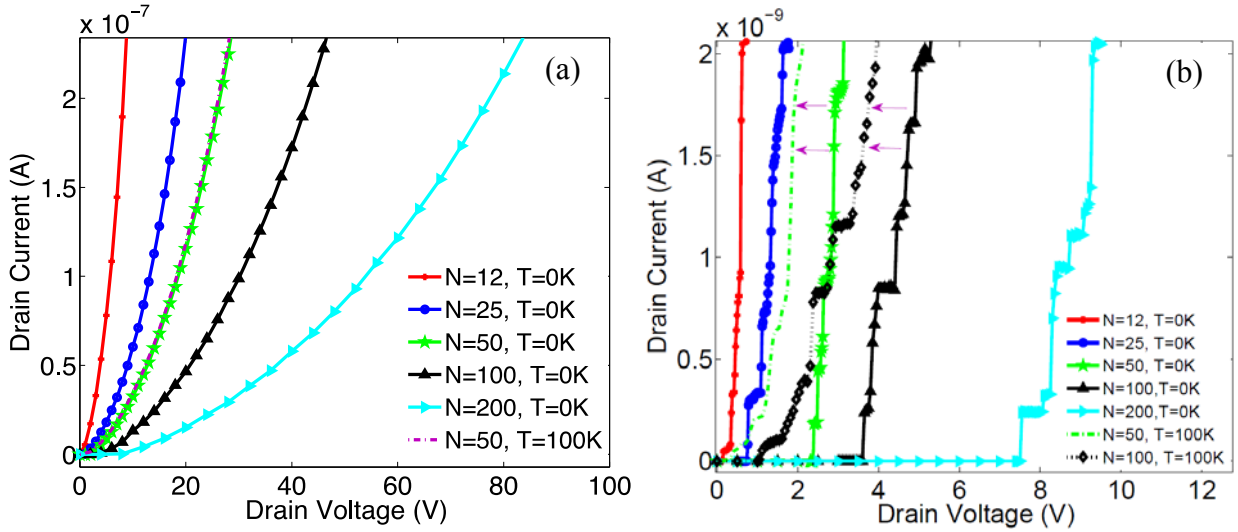

Figure 4. Simulated *IV* characteristics for the 1D chain of gold islands as a function of N, the number of islands in between the source and drain electrodes at $T = 0$ K. High bias results in (a), which also shows results for $N = 50$ at $T = 100$ K. Low bias results are shown in (b), highlighting the Coulomb Blockade and Coulomb staircase structures at $T = 0$ K and 100 K. Reprinted with permission from Savaikar *et al.* [10]. Copyright 2013, AIP Publishing LLC.

The effects of temperature on the *IV* characteristics are illustrated in figure 5. As shown in figure 5a, as the temperature is increased, the apparent threshold voltage drops, the Coulomb blockade structure seems to wash out, and the current increases at any given $V_{SD} > V_{th}$. Figure 5b illustrates the effects of temperature on the *IV* characteristics of a 25-junction device. At low temperatures, the $T = 0$ K turn-on threshold ($V_{th} \approx 0.74$ V) and the Coulomb staircases become rounded. As the temperature is increased, the apparent turn-on threshold voltage, the source-drain bias at which the current reaches some minimum detectable level, decreases. For $T \geq 40$ K, however, additional Coulomb staircase structures manifest themselves at voltages below the $T = 0$ K threshold voltage. For example, at $T = 40$ K a plateau develops in the current for drain voltages between ~0.35 V and 0.55 V. The currents associated with the plateaus of the Coulomb staircase steps also increase in magnitude with increasing temperature, while their widths correspondingly decrease.

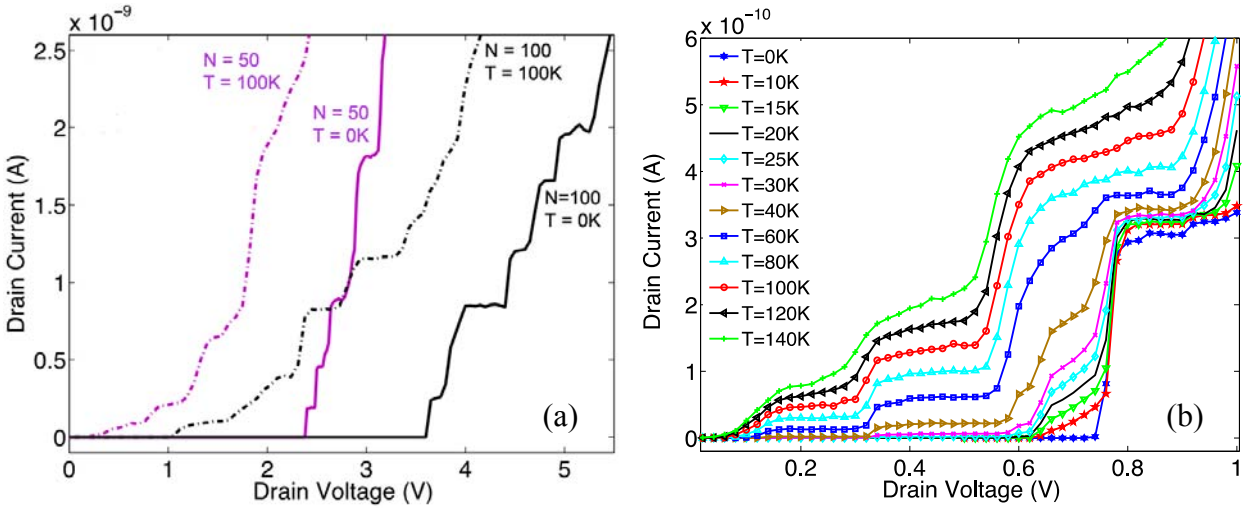

Figure 5. Simulated *IV* characteristics for a 1D chain as a function of temperature. (a) *IV* characteristics for two different chain lengths at $T = 0$ and $T = 100$ K. (b) *IV* characteristics for a device with $N = 25$ junctions at a series of temperatures between 0 and 140 K.

Two-dimensional devices

Experimental studies of 2D systems show *IV* characteristics with similar features to those observed in the 1D systems shown above, including a Coulomb blockade, Coulomb staircases, and non-linear *IV* relationships in the "on" state [4,20-23,26,27]. Preliminary investigations of two-dimensional (2D) random arrays of metallic nano-scale islands were carried out using MITS, and are briefly presented here in order to give a view of capabilities for future work.

Simulations of the 2D systems were carried out on a system of 67 spheres, each of diameter 6.5 nm. Positions of the islands were randomized using Metropolis Monte Carlo, which after decreasing all island diameters to 5.0 nm, resulted in a distribution of nearest-neighbor inter-island spacings ranging between ~1.5 to 5 nm (figure 6), and an average spacing of 2.7±0.1 nm. Simulations were carried out using MITS in the same manner as described above except that the island capacitances and junction capacitances were computed using finite-element methods. The junction capacitances between near-neighbor islands ranged between 1.5×10^{-20} to 10×10^{-20} F. Due to shielding effects from neighboring metallic islands, the island self-capacitances ranged from 0.6×10^{-20} to 4.0×10^{-20} F.

As shown in figure 6, currents tend to flow in the random 2D systems along a fairly narrow dominant conducting path, with many junctions carrying greater than 60% of the total current that is carried to the drain. With increasing V_{SD} (figure 6b) the DCP remained relatively robust, and some junctions in the DCP even increase the fraction of the current they carry. At low but non-zero temperatures (figure 6c), the DCP also remains robust.

The *IV* characteristic for the 67-island 2D device is shown in figure 7 for source-drain biases up to 2 V. The device shows a threshold voltage at ~1 V, and also a weak Coulomb staircase structure compared with the 1D devices. The inset in figure 7 shows the currents as a function of V_{SD} for each individual junction in the DCP. These *IV* curves show weak Coulomb staircase structures reminiscent of the total device *IV* behavior, as one might expect for a junction in a DCP.

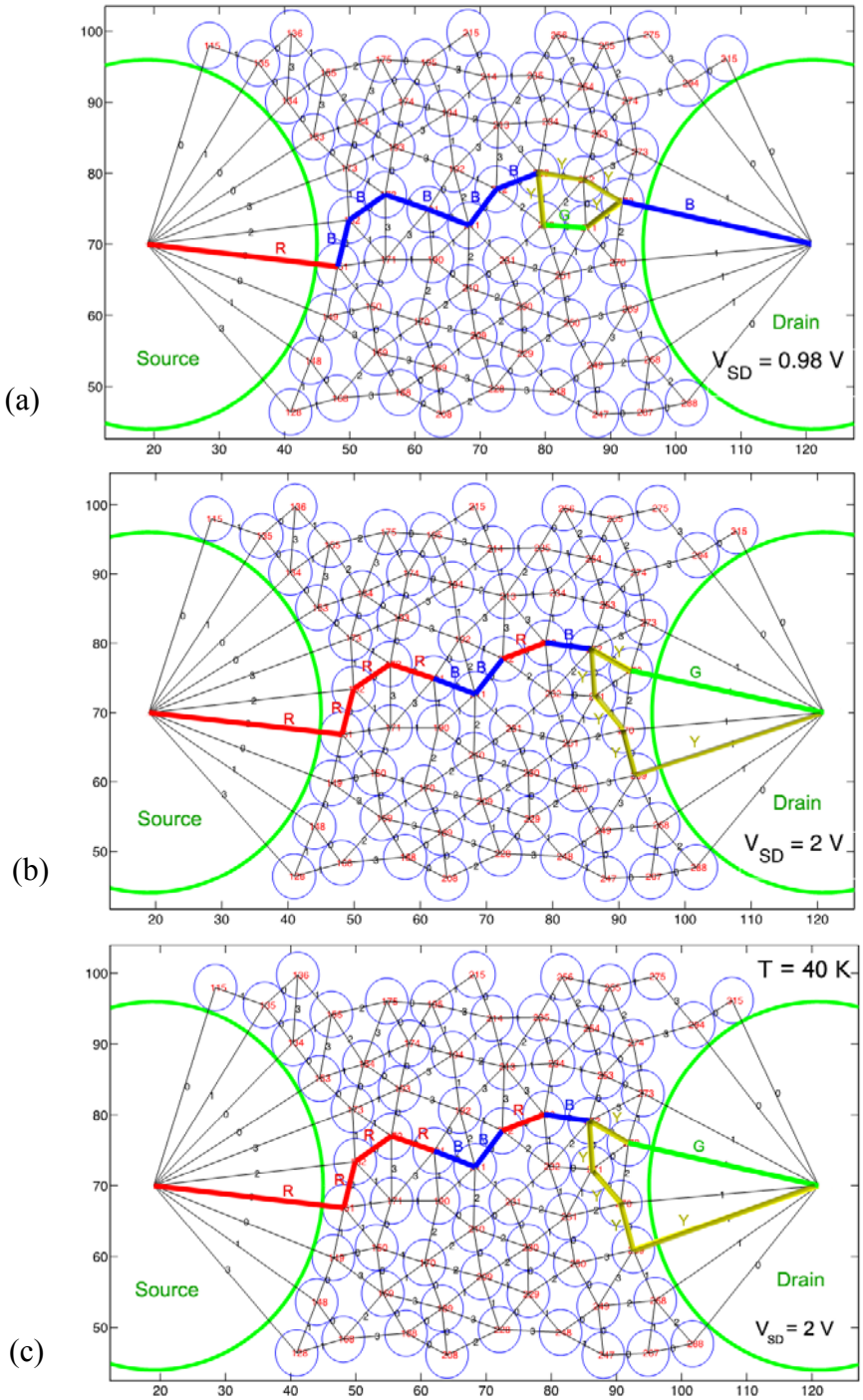

Figure 6. Schematic of a disordered 2D device consisting 67 islands, each of radius of 2.5 nm, randomly positioned on the plane between the source and the drain electrodes (large green ellipses) separated by ~50 nm. The nearest neighbor inter-island spacings range anywhere from ~1.5-5 nm. Allowed current paths are shown as solid black line segments. Junctions carrying significant current are color coded according to the percent of the total current carried to the drain: red (R) = 80-100%, blue (B) = 60-80%, green (G) = 40-60%, yellow (Y) = 20-40%. At T = 0 K as V_{SD} varies from 0.98 V (a) to 2 V (b), the DCP varies but largely retains its dominant conducting nature and position in the 2D array. (c) The same system at V_{SD} = 2V and T = 40K.

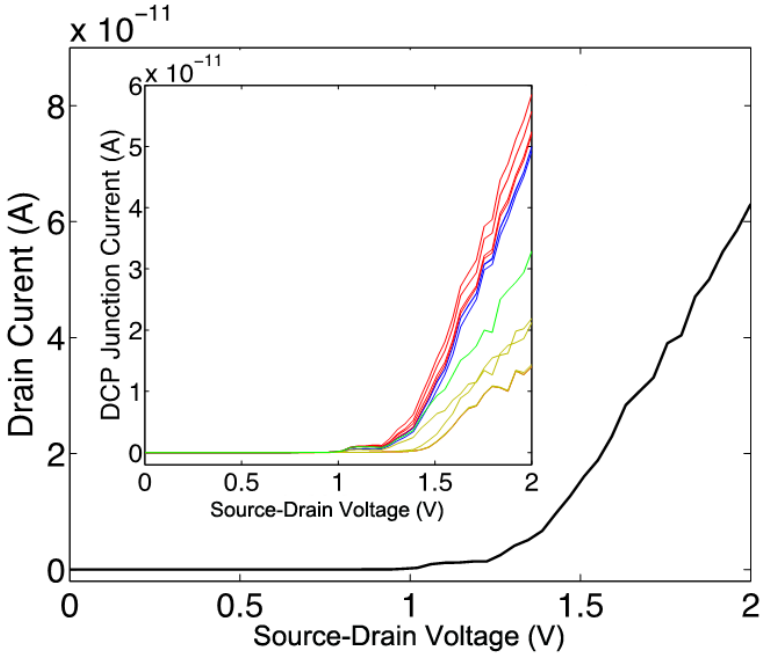

Figure 7. IV characteristics of a 2D device composed of 67 gold islands, as shown in figure 6, at $T = 0$ K, and in the absence of a gate voltage. The inset shows the distribution of currents flowing through individual junctions in the dominant conducting path as a function of applied source-drain voltage bias.

DISCUSSION

At any fixed V_{SD} in the on-state, the 1D devices show decreasing currents with increasing device length, as might be expected due to the increased overall resistance of the longer devices and associated increased number of resistive junctions. However, as demonstrated in figure 8, which shows the variation in the junction resistances as a function of junction width, the wider junctions in a device experience larger voltage drops across them. Because the barrier heights depend on the voltage drops across the junctions, the wider junctions also therefore experience a larger decrease in their tunneling resistances as the source-drain bias is increased (from 12 V to 80V).

MITS simulations demonstrate power-law behavior of the IV characteristics for V_{SD} beyond the threshold voltage, consistent with experiments. The non-Ohmic behavior ($\zeta > 1$), in the simulations has been traced to the dependence of the barrier heights on the voltage drops across the junctions, which varies with charge state and with V_{SD} . Whereas Middleton and Wingreen [24] have argued that ζ should equal 1 and 5/3 for infinite 1D and 2D systems, respectively, in the limit of short screening lengths (weak capacitive coupling among islands), their computer simulations for finite systems gave $\zeta = 1$ and 2.0 ± 0.2, respectively. A variety of experimental studies [23,25-28] give exponents ranging between 1 and 3.

Our simulation studies show that the exponent ζ is sensitive to the disorder in the system and the length of the device [10]. The exponents also show a crossover from a lower value to a higher value as the source-drain bias is increased sufficiently. Such crossover behavior has also been observed in experimental devices [25].

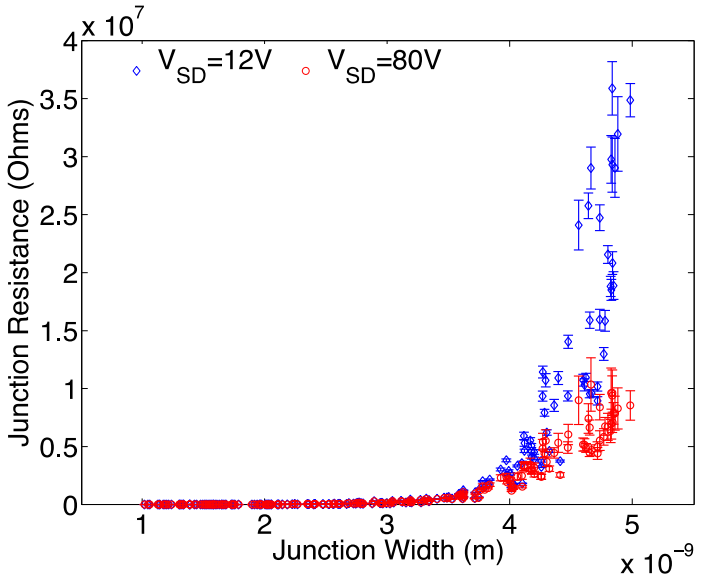

Figure 8. Junction resistances as a function of junction width, for a 200-junction device, for two different source-drain biases, 12 V (blue diamonds) and 80 V (red circles). Note from figure 4 that at 12 V the device is in the Coulomb-staircase regime, while at 80 V it is in the power-law regime. Error bars represent standard deviations in the junction resistances averaged over 5000 Monte Carlo steps (~1 ns at 12 V, and 18 ps at 80 V) after reaching steady state currents. Reprinted with permission from Savaikar *et al.* [10]. Copyright 2013, AIP Publishing LLC.

Values of the threshold voltage V_{th} increase with increasing device length; however, prediction of V_{th} for a device with random island sizes and separations is an open question. Although there is no steady state current for $V_{SD} < V_{th}$, as the applied voltage bias is increased across a device, but below the threshold, the charge state of the system changes in a discrete series of "up-steps" [23,24]. Based on our MITS simulations, these changes in charge state can include the following, alone or in combinations: (i) a change in total charge on the device, (ii) advancement of the charge front across the device, or (iii) rearrangement of charge among the islands. Such transitions occur when V_{SD} is increased sufficiently to bring some ΔW_{ij} to zero making a transition energetically favorable. For example, in a simulation of a 25-junction device, increases in V_{SD} necessary to overcome a total of 27 consecutive up-steps, as V_{SD} is increased from zero to V_{th}, range from 0.01 mV to 153.7 mV. Once a transition takes place, others may follow until once again the system reaches equilibrium. At sufficiently high bias, the last up-step may be overcome, and the ensuing transition will take place with some rate determined by Eq. 1. This transition is a rate-determining step, as a subsequent cascade of transitions then take place quickly, leading to the advancement of one net electron across the device, but ultimately leading to the system coming back to its rate-determining step. Unfortunately, prediction of the individual up-steps and V_{th}, based on a physical model of a 1D random device (materials, island radii, junction separations), appears to be impossible due to the capacitive junction couplings and dependence of the junction voltage drops on the charge state of the system and the applied bias.

With increasing V_{SD} beyond V_{th}, the currents change only slowly due to the slight changes in the junction voltage drops, that is, until some particular $V_{i'j'}$ reaches a value such that its associated $\Delta W_{i'j'}$ reaches zero and the charge state of the system changes. This can lead to the creation of a new conduction channel (sequence of allowed transitions in charge-state- V_{SD} space that results in a net transfer of charge across the device), leading to a sharp increase in the current

and the formation of a step in the CS. With increasing V_{SD}, ever more conduction channels open up, until at sufficiently high V_{SD} the individual CS steps become indistinguishable.

With increasing temperature, key ΔW_{ij} activation barriers for changes in charge state can be thermally overcome that lead to changes in charge state and to non-zero transition rates, even for $V_{SD} < V_{th}$. Thus, thermal effects can lead to a non-linear decrease of the apparent threshold voltage of a device with increasing temperature, and rounding or elimination of steps in the CS structure. New CS steps can even manifest themselves $V_{SD} < V_{th}$ due to the system attaining charge states at non-zero temperatures that are inaccessible at $T = 0$ and $V_{SD} < V_{th}$. Further details of thermal effects in random 1D devices will be the subject of a future publication.

In experimental work on a 2D system of Au grains, by Cordan *et al.* [4] postulated the existence of a quasi-1D dominant conducting path (DCP) that carried most of the current across devices with a wide range of tunneling resistances. Our preliminary work using MITS has demonstrated the existence of a DCP in a random 2D device. The DCP shows robustness with changes in source-drain voltage and with moderate increases in temperature. The Coulomb staircase structure in the 2D device was less pronounced than in comparable 1D systems, however. This is likely due to the DCP being relatively optimized, and thus carrying a narrower range of tunneling resistances along the DCP than which exists among neighboring junctions in the overall 2D device. Our preliminary 2D simulations were also carried out on a relatively small system, leading to a short path length for the DCP. As shown above, the Coulomb staircase structure becomes less prominent as the device length decreases due to shorter devices having a lower probability of sampling unusually large junction widths.

CONCLUSIONS

The MITS simulation package has proven to be a useful tool for modeling *IV* characteristics of 1D and 2D arrays of nano-scale metallic islands under low and high biases, and gaining understanding of underlying mechanisms to explain the Coulomb blockade, Coulomb staircase, and power-law scaling behavior of the devices. The turn-on threshold source-drain bias depends strongly on the capacitances of the system, but because of the inherent randomness in island spacing and radii, the prediction of the threshold voltage based on the physical layout of a random device is not possible without carrying out the full simulation. With increasing source-drain bias the threshold is reached through a series of up-steps in which the charge state of the system changes, and the charge front eventually advances across the device. In agreement with the hypothesis of Cordan *et al.* [4], 2D systems with sufficient disorder have a robust dominant conducting path that carries most of the current across the device.

Future studies are planned to elucidate the effects of temperature and degree of randomness on the behavior of such systems. Such insights may be helpful in using MITS to explore device designs with the goal of engineering desired device characteristics.

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